## PATENT COOPERATION TREATY

# TRANSLATION INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

A 1' 4'	1							
Applicant's or agent's file reference P33546-P0	FOR FURTHER ACTION		See Form PCT/IPEA/416					
International application No.	International filing date (da	av/month/year)	Priority date (day/month/year)					
	17.05.2004	03.10.2003						
PCT/JP2004/007006			03.10.2003					
International Patent Classification (IPC) or national classification and IPC								
G06F17/50, H01L21/82, H03K19/00								
Applicant  MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.								
<ol> <li>This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.</li> </ol>								
2. This REPORT consists of a total o	5	sheets, including	this cover sheet.					
3. This report is also accompanied by	ANNEXES, comprising:							
<u> </u>	nd to the International Bureau,	) a total of 35	sheets, as follows:					
1			mended and are the basis for this report and/or					
sheets of the description, claims authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).								
sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental								
	Box.							
b (sent to the Internation	b. (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s))							
	, containing a sequence listing and/or tables							
related thereto, in composed Section 802 of the Admir		icated in the Suppler	mental Box Relating to Sequence Listing (see					
This report contains indications re			<del>-</del>					
l								
Box No. I Basis of	he report							
Box No. II Priority								
Box No. III Non-esta	blishment of opinion with rega	ard to novelty, inventi	ive step and industrial applicability					
Box No. IV Lack of	Box No. IV Lack of unity of invention							
Box No. VI Certain o								
Box No. VII Certain	Box No. VII Certain defects in the international application							
Box No. VIII Certain observations on the international application								
			is amount					
Date of submission of the demand	Date	e of completion of thi	istopoli					
Name and mailing address of the IDEA/ID		harinad off						
Name and mailing address of the IPEA/JP		horized officer						
Facsimile No.	Tele	phone No.						

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International application No.
PCT/JP2004/007006

Box	No. I	Basis of the report							
1.		regard to the language, this report is based on the internation ated under this item.	nal application in the language in w	thich it was filed, unless otherwise					
	This report is based on translations from the original language into the following language which is the language of a translation furnished for the purposes of:								
		international search (Rule 12.3 and 23.1(b))	international search (Rule 12.3 and 23.1(b))						
		publication of the international application (Rule 12.4)	•						
		international preliminary examination (Rule 55.2 and/	or 55.3)						
2.	recei	With regard to the elements of the international application, this report is based on (replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report):							
	$\mathbb{H}$	the international application as originally filed/furnished							
		the description:							
		pages 1-4, 6, 15-17, 20-67		as originally filed/furnished					
		pages* 5, 5/1, 7-14, 18-19/1							
	_	pages*	received by this Authority on _						
	$\bowtie$	the claims:							
		nos. 2-6, 8, 9, 11, 12, 15, 17, 21, 23,	26-34, 38-40	as originally filed/furnished					
		nos.*	as amended (together	with any statement) under Article 19					
		nos.* 25, 35-37	received by this Authority on _	18.03.2005					
		nos.*	received by this Authority on						
	$\boxtimes$	the drawings:							
		sheets fig. 1-38		as originally filed/furnished					
		sheets*	received by this Authority on						
		sheets*	received by this Authority on						
		a sequence listing and/or any related table(s) - see Supplem	ental Box Relating to Sequence Lis	sting.					
3.	$\boxtimes$	The amendments have resulted in the cancellation of:							
		the description, pages		_					
		the claims, nos. 13							
		the drawings, sheets/figs							
		any table(s) related to sequence listing (specify):							
4.		This report has been established as if (some of) the amend they have been considered to go beyond the disclosure as fi							
		the description, pages							
		the claims, nos.	· · · · · · · · · · · · · · · · · · ·						
			the drawings, sheets/figs						
		the sequence listing (specify):							
		any table(s) related to sequence listing (specify):							
*	If ite	m 4 applies, some or all of those sheets may be marked "sup	erseded."						

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Box	No. V Reasoned statement citations and expla			h regard to novelty, inventive step or industrial applicability;	
1.	Statement				
	Novelty (N)	Claims	1-12,	14-40	YES
		Claims			NO
	Inventive step (IS)	Claims	1-12,	14-40	YES
		Claims			NO
	Industrial applicability (IA)	Claims	1-12,	14-40	YES
		Claims			NO

- 2. Citations and explanations (Rule 70.7)
  - Document 1: JP 2001-160622 A (NEC Corp.), 12 June 2001, claims 1 and 5 & US 2001/0002707 A1
  - Document 2: JP 10-301983 A (NEC Corp.), 13 November 1998, abstract, paragraph [0015] and fig. 4 and 5 (Family: none)
  - Document 3: JP 8-194726 A (Fujitsu Ltd.), 30 July 1996, paragraphs [0006] to [0007] and claim 2 & US 5706477 A

Explanations

Document 1 discloses a technique that employs a model wherein a resistor (and a voltage controlled current source) has (have) been inserted between the gate and the drain as well as between the gate and the source.

However, the reasons for the insertion of the resistors and the sites where the resistors are inserted in the model that is disclosed in document 1 are different from the reasons and the sites in the inventions that are set forth in claims 1 to 12 and 14 to 40 of the present application.

Document 2 discloses a technique that employs the resistor (r1), the resistor (r2), the resistor (Rp) and

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Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

the resistor (Rd) when carrying out power consumption calculations that reflect both the through current and the leak current; however, the reasons for the insertion of the resistors and the sites where the resistors are inserted in the technique that is disclosed in document 2 are different from the reasons and the sites in the inventions that are set forth in claims 1 to 12 and 14 to 40 of the present application.

Document 3 discloses a technique whereby the logic information and the wiring information are converted into a circuit model using the sub-circuits that have been stored in the sub-circuit storage unit in order to reduce the number steps that are necessary for the creation of a simulation model; however, the technique in question does not involve the insertion of resistors, and thus differs from the inventions that are set forth in claims 1 to 12 and 14 to 40 of the present application.

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Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

With regards to the invention set forth in claim 1, it is impossible to specify the relationship (e.g. the proportion or the like) of the resistance value of the resistance element that is inserted into the power source side and the resistance value of the resistance element that is inserted into the reference electric potential side. As a result, it is impossible to specify the resulting electric potential of the gate terminal during an analysis of the invention in question. Such being the case, the technical significance of the insertion of the resistance elements is unclear in the light of the disclosure in claim 1. In addition, the relationship between the insertion of the resistors and the detection of the through current is also unclear. The same is true with regards to the other claims.